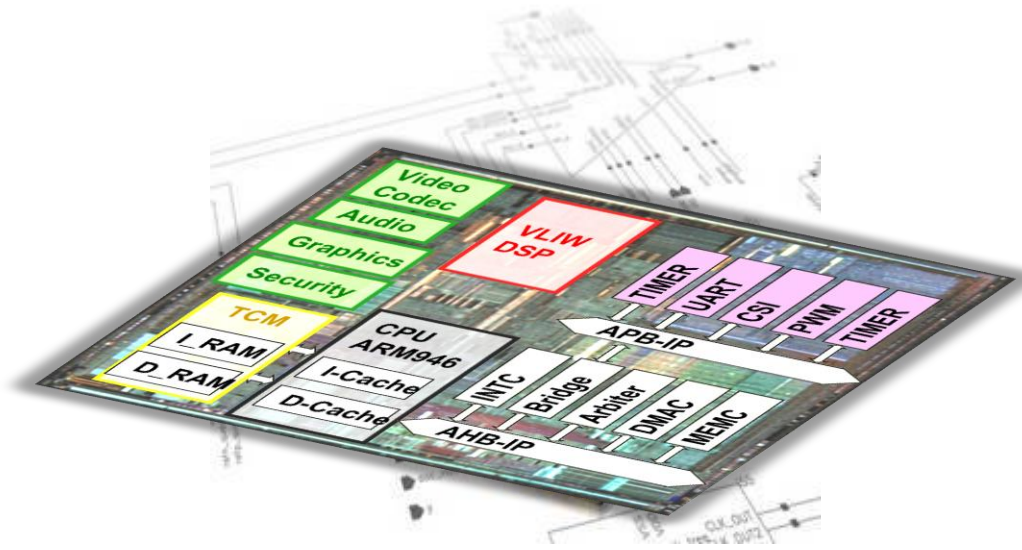


ECE 695R: System-on-Chip Design

Module 1 (Lectures 1-3): Course Introduction and Background



Anand Raghunathan
MSEE 348
raghunathan@purdue.edu

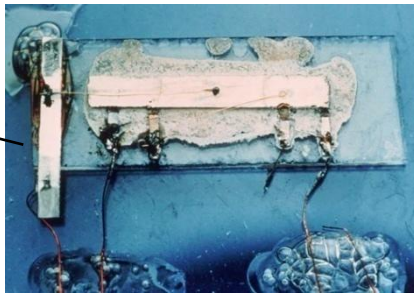
Fall 2011, EE 115, T Th 4:30PM-5:45PM

Lecture #1

- Introduction and context for the course
 - Moore's Law drives system-level integration
 - SoCs: What & Why?
 - Key design issues
- Course description
 - Topics covered
 - Expected background
 - Hands-on assignments and project
 - Grading
 - Logistics

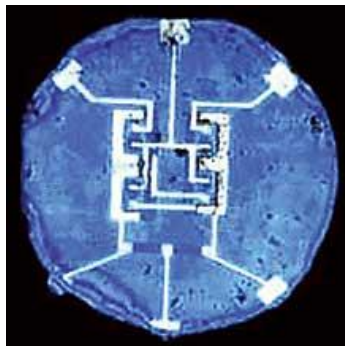
A Brief History of Integrated Circuits

1 Transistor
3 Resistors
1 Capacitor



Germanium IC
Jack Kilby
Texas Instruments

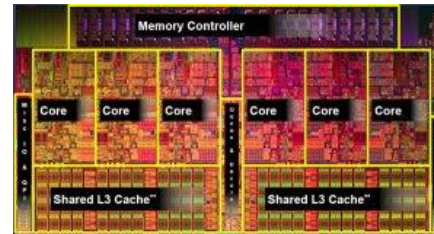
From



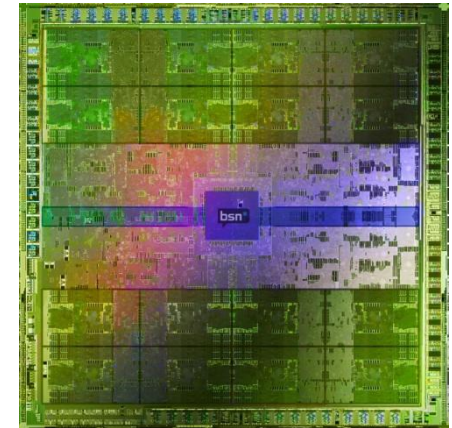
Silicon IC
Robert Noyce
Fairchild
Semiconductor

circa 1958

To



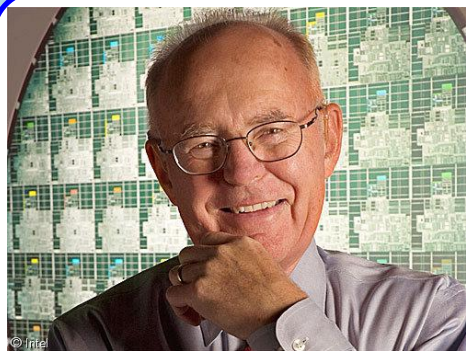
Intel Gulftown (six-core
microprocessor)
1.17 Billion transistors
(32 nm)



NVIDIA GTX580
(Graphics processor
with 512 "cores")
3.05 Billion transistors
(40 nm)

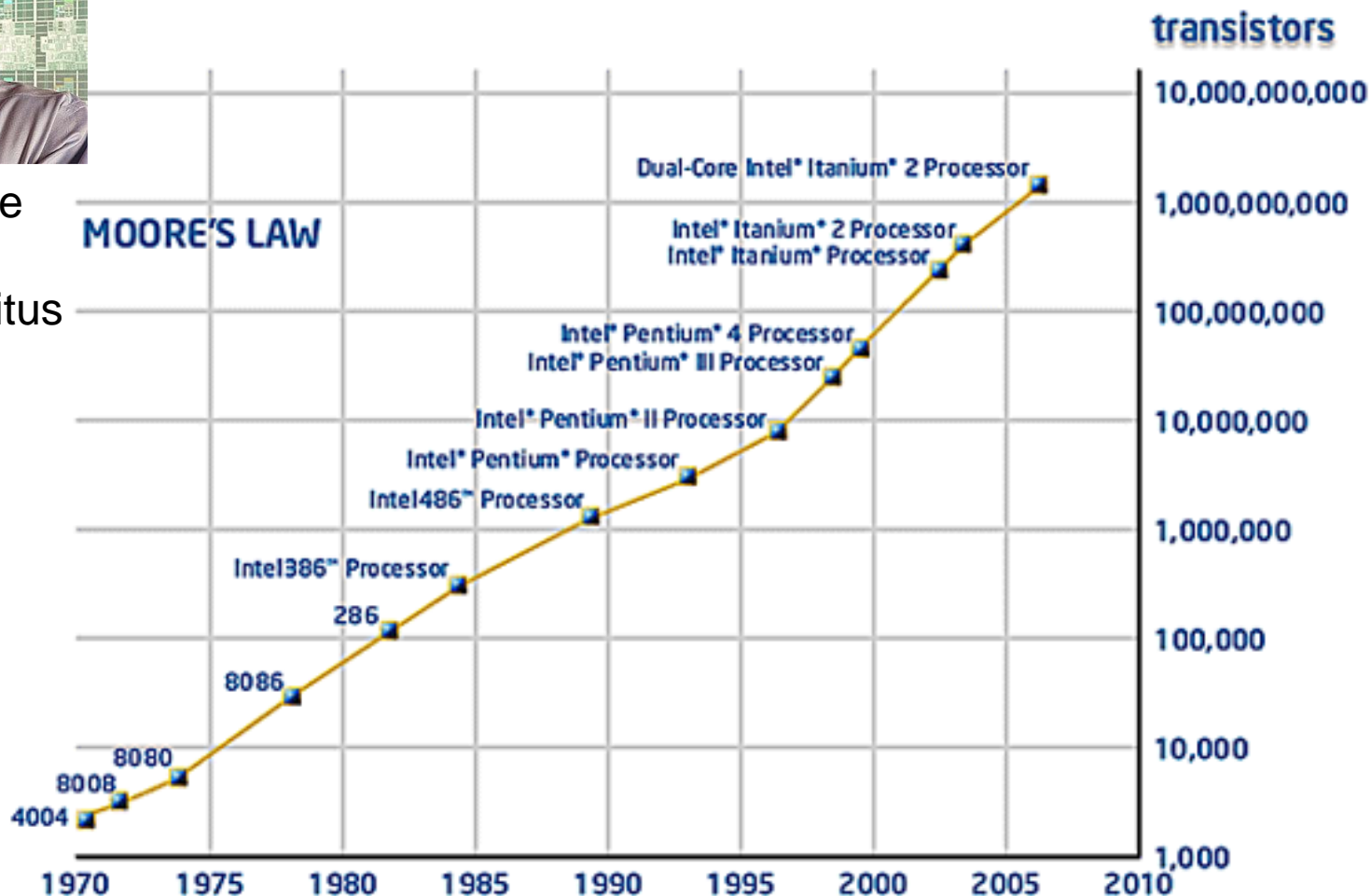
circa 2011

A 1,500,000,000 fold
increase in 50 years



Moore's Law

Gordon E. Moore
Co-founder and
Chairman Emeritus
Intel



- An empirical observation (and prediction) of the growth in number of transistors in integrated circuits over time

Source: intel.com

Moore's Law ... in his own words

The future of integrated electronics is the future of electronics

itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home Computers – or at least terminals connected to a central computer – automatic controls for automobiles, and personal portable communications equipment.

....

....

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wrist-watch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the

machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

The author



Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Moore's Law ... in his own words

....

....

For simple circuits, the cost per component is nearly inversely proportional to the number of components, the result of the equivalent piece of semiconductor in the equivalent package containing more components. But as components are added, decreased yields more than compensate for the increased complexity, tending to raise the cost per component. Thus there is a minimum cost at any given time in the evolution of the technology.

....

....

The establishment

Integrated electronics is established today. Its techniques are almost mandatory for new military systems, since the reliability, size and weight required by some of them is achievable only with integration. Such programs as Apollo, for manned moon flight, have demonstrated the reliability of integrated electronics by showing that complete circuit functions are as free from failure as the best individual transistors.

Most companies in the commercial computer field have machines in design or in early production employing integrated electronics. These machines cost less and perform better than those which use "conventional" electronics.

Instruments of various sorts, especially the rapidly increasing numbers employing digital techniques, are starting to use integration because it cuts costs of both manufacture and design.

The use of linear integrated circuitry is still restricted primarily to the military. Such integrated functions are expensive and not available in the variety required to satisfy a major fraction of linear electronics. But the first applications are beginning to appear in commercial electronics, particularly in equipment which needs low-frequency amplifiers of small size.

Reliability counts

In almost every case, integrated electronics has demonstrated high reliability. Even at the present level of production—low compared to that of discrete components—it offers reduced systems cost, and in many systems improved performance has been realized.

Integrated electronics will make electronic techniques more generally available throughout all of society, performing many functions that presently are done inadequately by other techniques or not done at all. The principal advantages will be lower costs and greatly simplified design—payoffs from a ready supply of low-cost functional packages.

For most applications, semiconductor integrated circuits will predominate. Semiconductor devices are the only reasonable candidates presently in existence for the active elements of integrated circuits. Passive semiconductor elements look attractive too, because of their potential for low cost and high reliability, but they can be used only if precision is not a prime requisite.

Silicon is likely to remain the basic material, although others will be of use in specific applications. For example, gallium arsenide will be important in integrated microwave functions. But silicon will predominate at lower frequencies because of the technology which has already evolved around it and its oxide, and because it is an abundant and relatively inexpensive starting material.

Costs and curves

Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate. For simple circuits, the cost per component is nearly inversely proportional to the number of components, the result of the

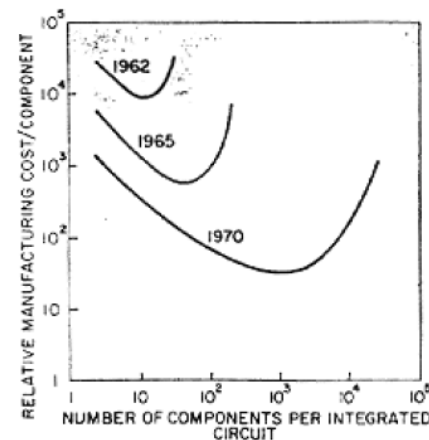
equivalent piece of semiconductor in the equivalent package containing more components. But as components are added, decreased yields more than compensate for the increased complexity, tending to raise the cost per component. Thus there is a minimum cost at any given time in the evolution of the technology. At present, it is reached when 50 components are used per circuit. But the minimum is rising rapidly while the entire cost curve is falling (see graph below). If we look ahead five years, a plot of costs suggests that the minimum cost per component might be expected in circuits with about 1,000 components per circuit (providing such circuit functions can be produced in moderate quantities.) In 1970, the manufacturing cost per component can be expected to be only a tenth of the present cost.

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph on next page). Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.

I believe that such a large circuit can be built on a single wafer.

Two-mil squares

With the dimensional tolerances already being employed in integrated circuits, isolated high-performance transistors can be built on centers two thousandths of an inch apart. Such



Moore's Law ... in his own words

....
....

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph). Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.

....



a two-mil square can also contain several kilohms of resistance or a few diodes. This allows at least 500 components per linear inch or a quarter million per square inch. Thus, 65,000 components need occupy only about one-fourth a square inch.

On the silicon wafer currently used, usually an inch or more in diameter, there is ample room for such a structure if the components can be closely packed with no space wasted for interconnection patterns. This is realistic, since efforts to achieve a level of complexity above the presently available integrated circuits are already underway using multilayer metalization patterns separated by dielectric films. Such a density of components can be achieved by present optical techniques and does not require the more exotic techniques, such as electron beam operations, which are being studied to make even smaller structures.

Increasing the yield

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as

is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations that often limit yields in chemical reactions; it is not even necessary to do any fundamental research or to replace present processes. Only the engineering effort is needed.

In the early days of integrated circuitry, when yields were extremely low, there was such incentive. Today ordinary integrated circuits are made with yields comparable with those obtained for individual semiconductor devices. The same pattern will make larger arrays economical, if other considerations make such arrays desirable.

Heat problem

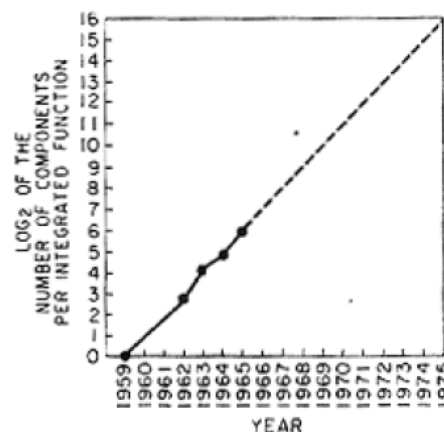
Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?

If we could shrink the volume of a standard high-speed digital computer to that required for the components themselves, we would expect it to glow brightly with present power dissipation. But it won't happen with integrated circuits. Since integrated electronic structures are two-dimensional, they have a surface available for cooling close to each center of heat generation. In addition, power is needed primarily to drive the various lines and capacitances associated with the system. As long as a function is confined to a small area on a wafer, the amount of capacitance which must be driven is distinctly limited. In fact, shrinking dimensions on an integrated structure makes it possible to operate the structure at higher speed for the same power per unit area.

Day of reckoning

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large



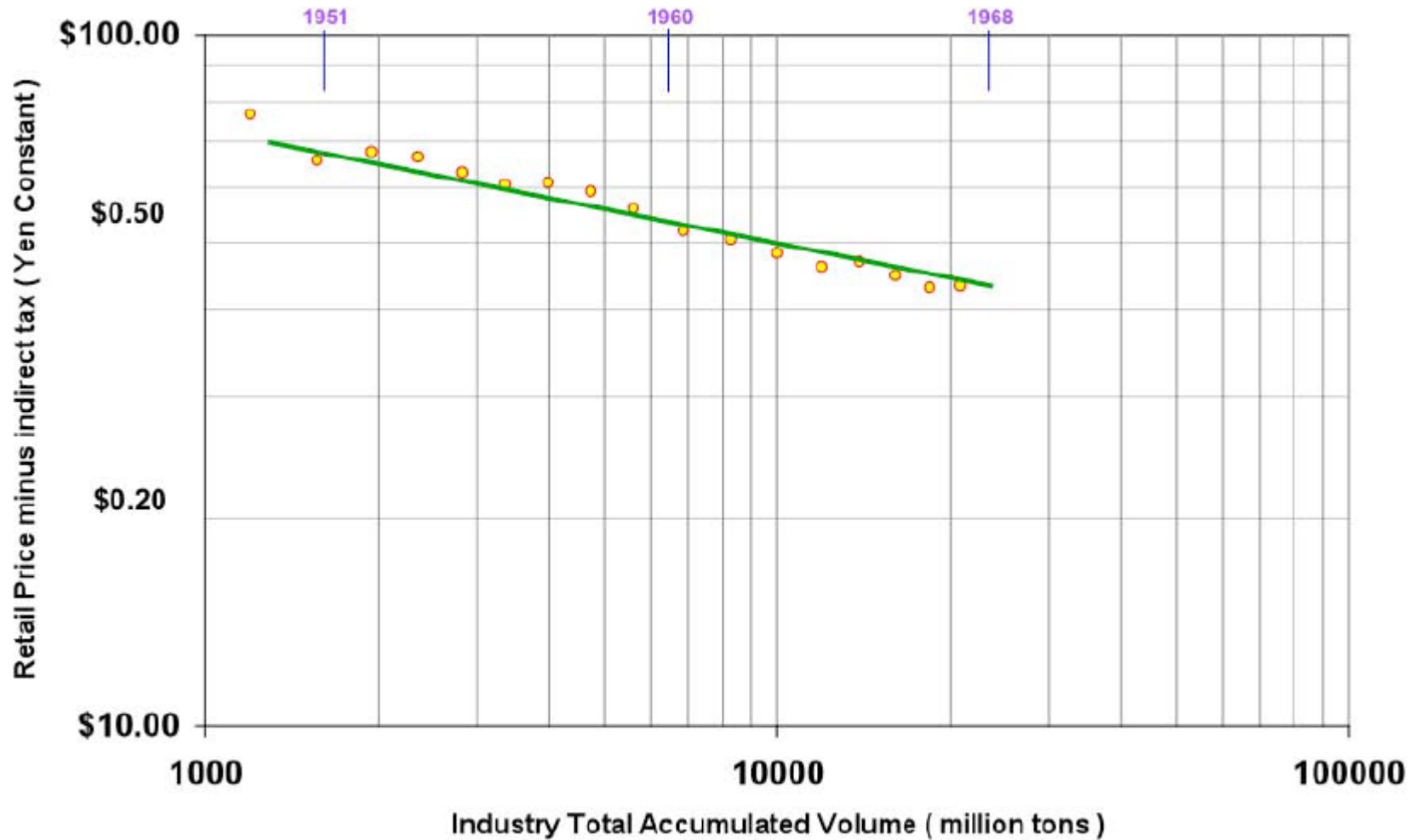
Moore's Law is Based on the Concept of "Learning Curve"



- **Cost per unit decreases by a fixed percent every time total cumulative volume doubles**
- **Applies to all free market products and services (over centuries) when measured in constant currency**
- **Used to predict future costs**
 - Aircraft industry
 - Semiconductor industry
- **Also true for subsystem or component costs and improvements in reliability, quality, yield, etc.**

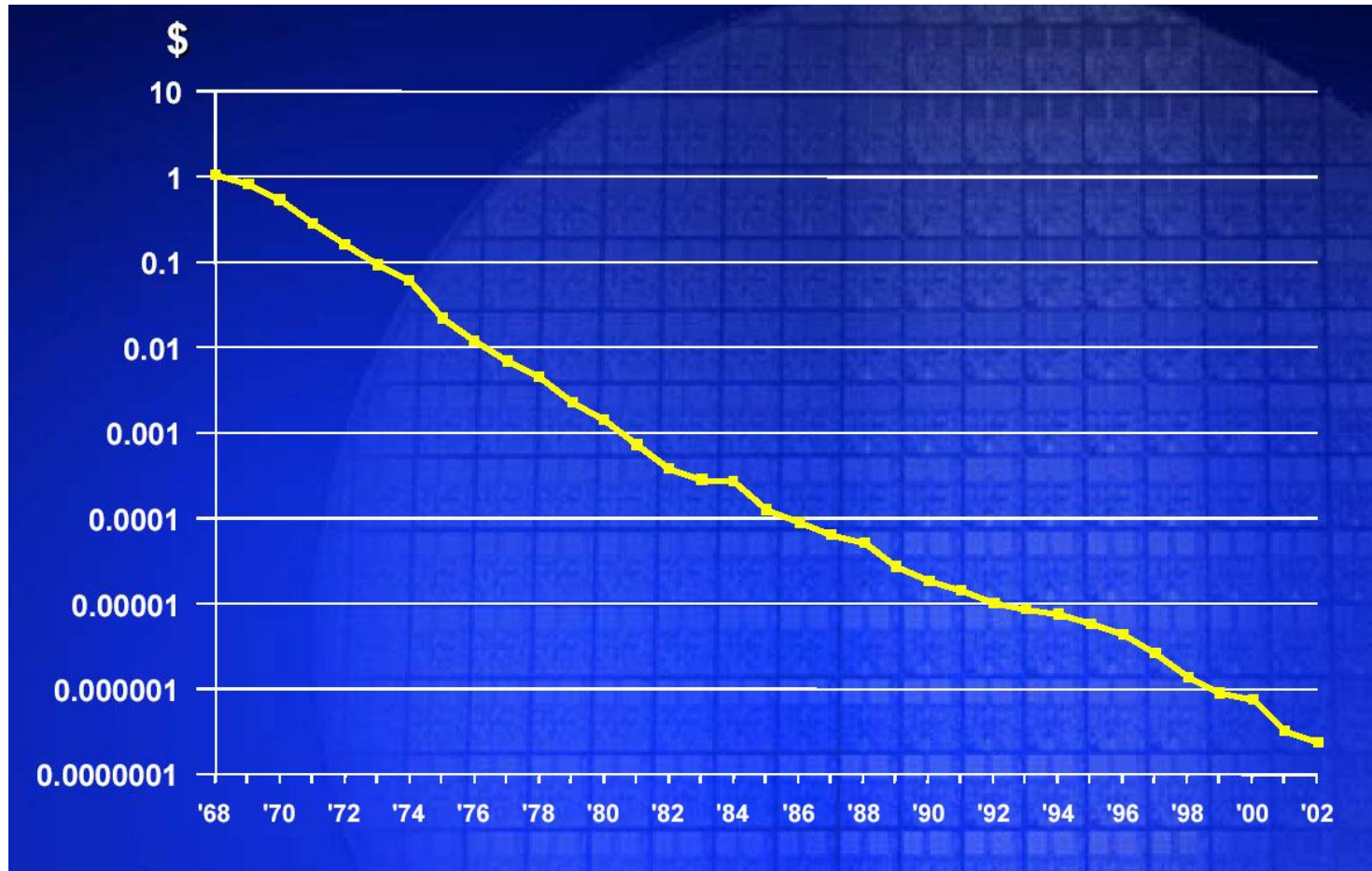
Source: Walden Rhines, Keynote presentation, VLSI Design Conference 2010

Learning Curve for Japanese Beer



Source: Boston Consulting Group

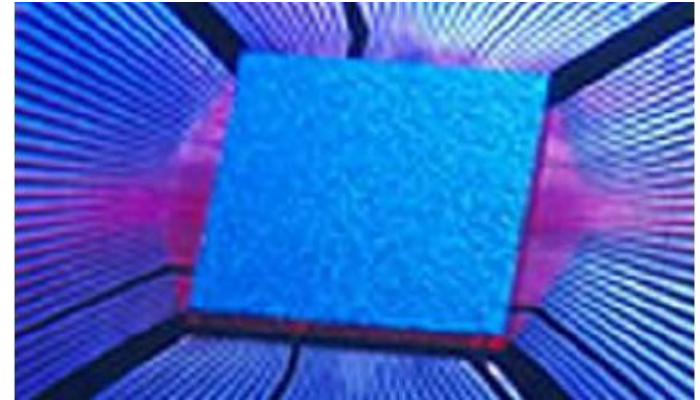
Learning Curve for Integrated Circuits



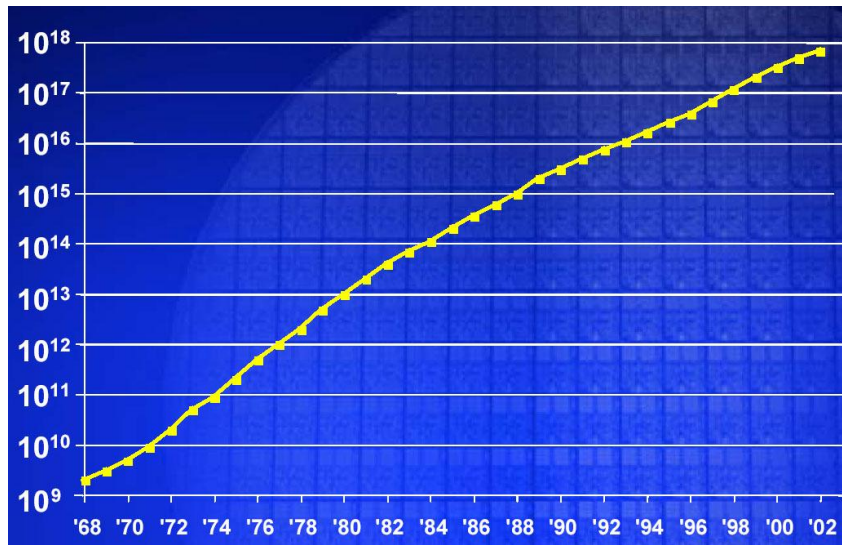
Source: Intel

Hooray, we're drowning in.... Transistors!

- Ten quintillion: 10^{18}
 - ~ The number of transistors shipped in 2004!
 - > The estimated number of grains of rice harvested in 2004
 - 100 times estimated number of ants on earth



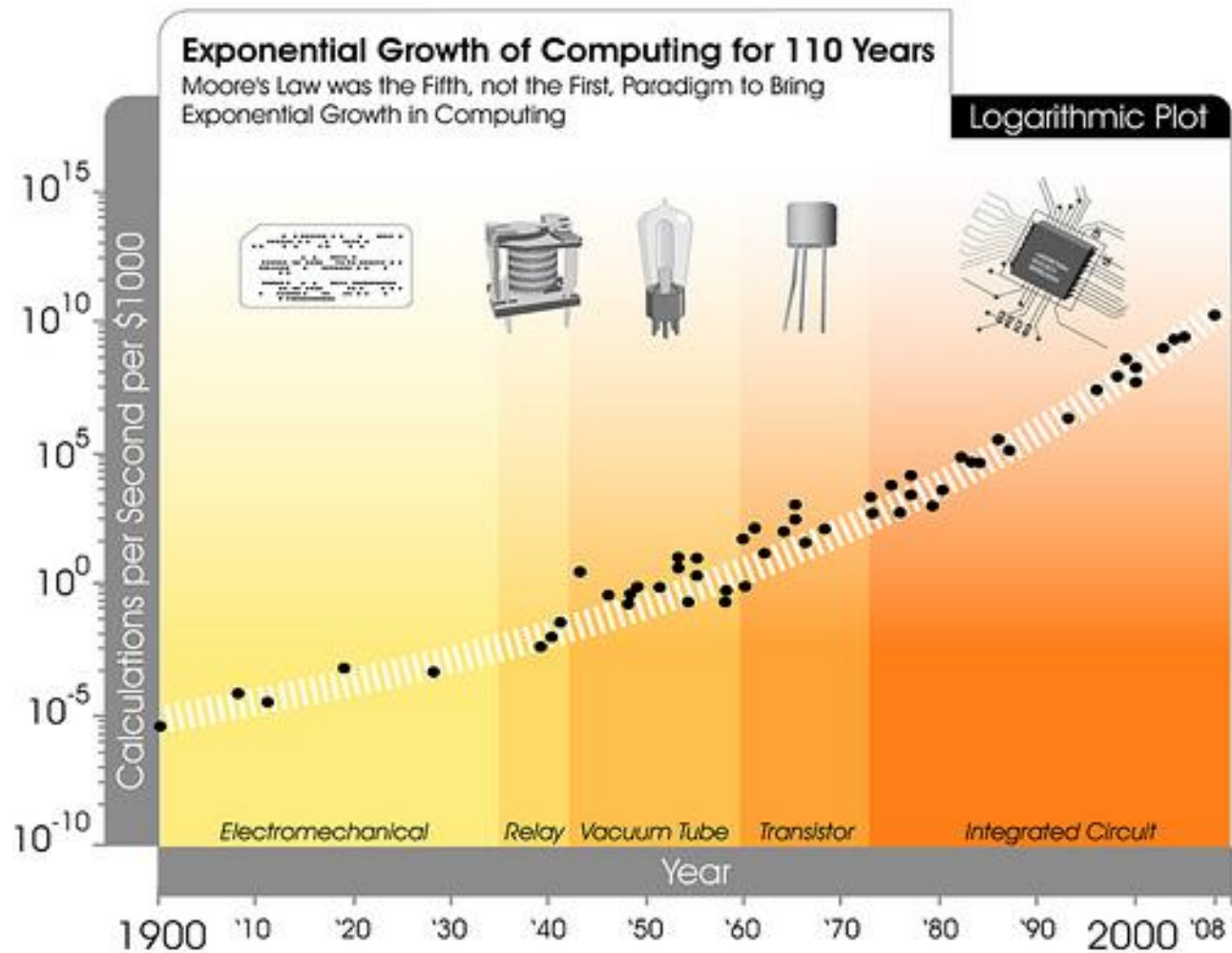
Transistors shipped worldwide



Sources: "A Law of Continuing Returns", Los Angeles Times, April 17 2005
ISSCC 2004 Keynote, Gordon Moore

Moore's Law: The fifth paradigm

- Increasing compute performance to cost ratios for over 100 years



Source: Ray Kurzweil

What do we do with all the transistors?

- Option #1 (general-purpose products)
 - Microprocessors, GPUs
 - Pre-2005: Deeper pipelines, more complex logic for instruction-level parallelism, more cache
 - 2005- : More cores, more cache
 - Memory chips
 - Easy – just keep increasing capacity
 - ???

What do we do with all the transistors?

- Option #2 (98 % of “computing” systems)
 - Integrate more and more system functions onto a chip

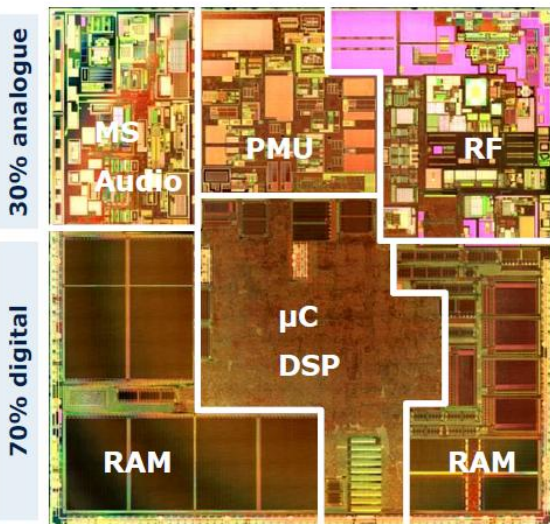


- Benefits of integration
 - Size (miniaturization)
 - Cost
 - Performance
 - Power

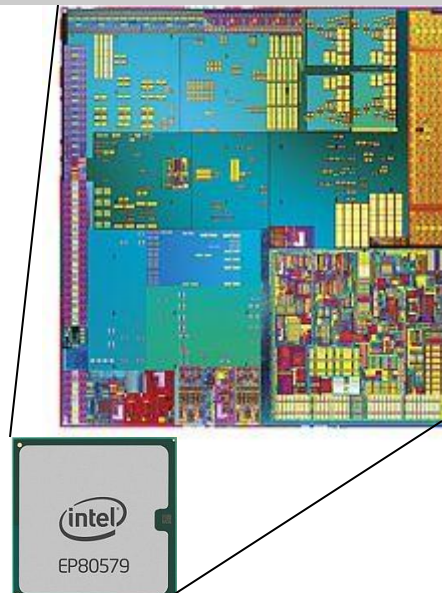
What are Systems-on-chip?

- Direct consequence of increasing scales of integration (Moore's Law)
 - Integrate hitherto discrete system components into a single chip
 - Tremendous benefits in cost, size, performance, power consumption

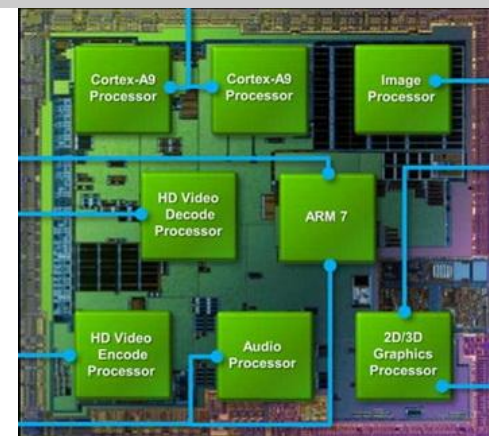
Infineon E-GOLDVoice
“Phone-on-a-chip”



Intel EP80579 SoC for
embedded systems
(security,
communications, storage)



NVIDIA Tegra2 SoC for
tablets, slates, e-readers,
MIDs, set-top boxes



What are Systems-on-chip?

- Large and growing market - \$35B in 2007, ~20% CAGR

ards Memory Video Storage Multimedia Cooling Cases/PSU Monitors Networking Mobile Other

News

Intel to Ship More System-on-Chip Devices than Microprocessors – Chief Executive.

Intel Expects Demand Towards SoCs to Increase

[09/23/2009 06:56 AM]
by [Anton Shilov](#)

Paul Otellini, chief executive officer at Intel Corp., said that the demand towards system-on-chip (SoC) devices was set to grow and that at some point in future Intel would ship more SoCs than microprocessors. At present Intel pins a lot of hopes on SoCs featuring Atom processing cores, which means that such devices will hardly offer truly high computing performance.

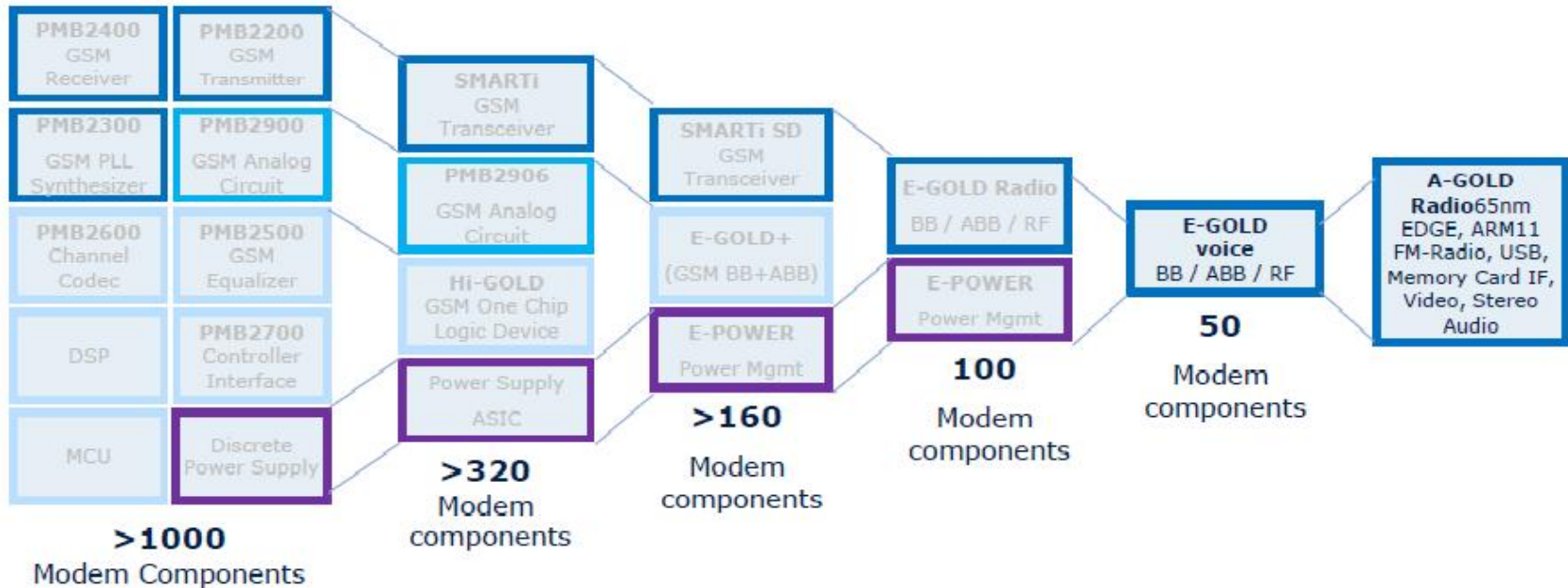
"We already have over twelve 32nm SoCs in development at Intel coming out over the next couple of years. And, in fact, if I look forward, out, say, five years or so, I can easily see the point where Intel Corporation ships more SoC devices per year than standard microprocessors," said Paul Otellini during his keynote at Intel Developer Forum 2009.

It is rather logical for Intel to concentrate on system-on-chip devices: the vast majority of SoCs power miniature electronics, including mobile Internet devices, portable digital media players, video game consoles, consumer electronics, embedded applications, communication equipment, cell phones, in-car entertainment systems and many other types of computing devices. The total available market for SoCs is naturally considerably higher compared to that of central processing units (CPUs).

At present low power electronics is based on ARM microprocessors developed by various

Benefits of SoC Integration: Size

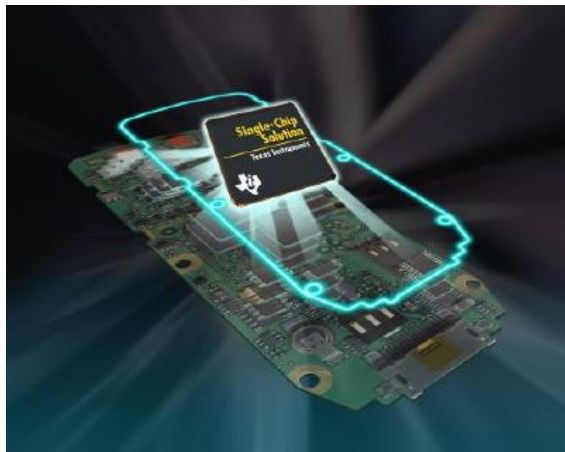
- Impact of SoCs on mobile phones



Source: Hermann Eul, Infineon

Benefits of SoC Integration: Cost

- “Single-chip” cell phone



Munich, Germany and Barcelona, Spain – February 13, 2006

“....

The latest chip from Infineon Technologies AG (FSE/NYSE: IFX) reduces the number of electronic components in a basic mobile phone from about 100 to fewer than 50.

...

Infineon's E-GOLDvoice™ single-chip solution combines a baseband processor, radio frequency transceiver, power management unit and RAM in a footprint measuring just 1.5mm x 1.5mm, setting a new record level of silicon integration for mobile communications...

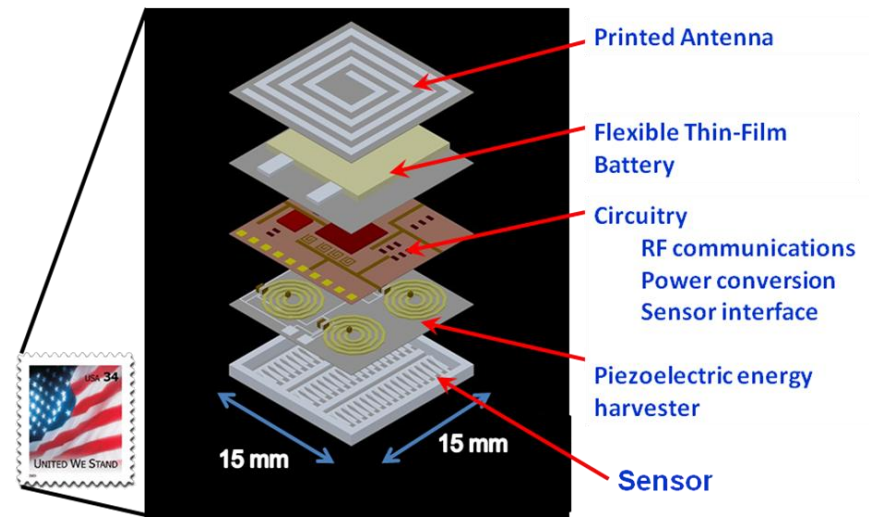
Spice Mobile has launched a “people’s phone” for under \$20... Globally, over 20% of the mobile phone market is represented by the ultra low cost segment.



Source: TI, Nokia, Infineon

Benefits of Integration: Size/Cost

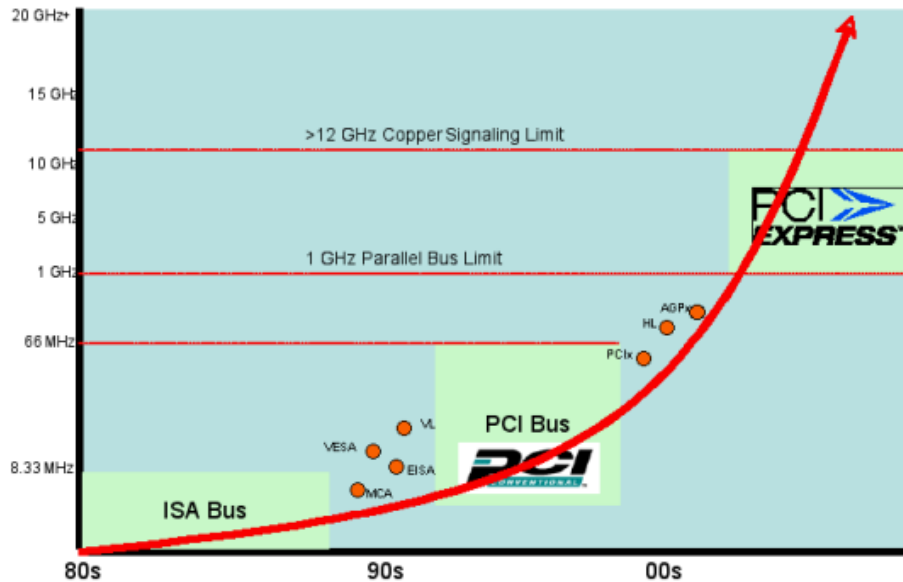
- Extreme size constraints
 - Integrated sensors for structural (building, bridge, aircraft) monitoring
 - Biomedical implants



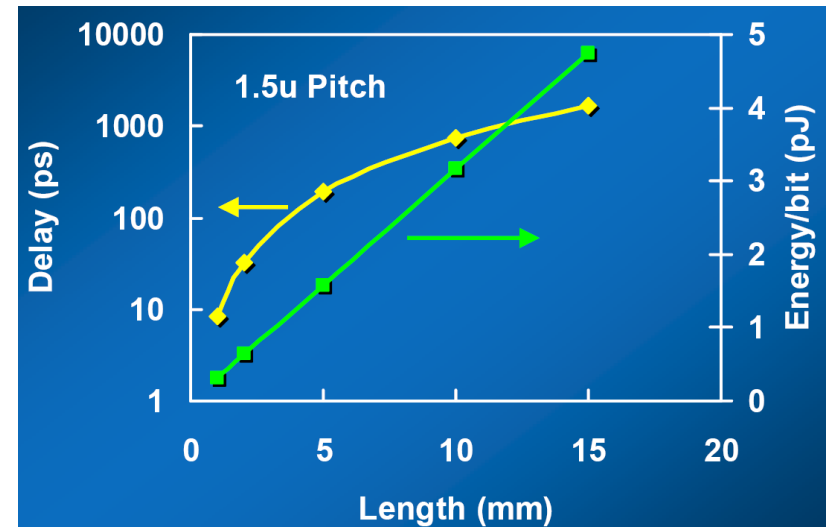
Integrated sensor for aircraft structural monitoring - conceptual design (Courtesy Prof. Byunghoo Jung, Prof. Dimitri Peroulis)

Benefits of Integration: Performance/Power

- Integration converts off-chip traffic into on-chip traffic
 - Off-chip communication: $\sim 1\text{-}10\text{GB/s}$, $\sim 1\text{nJ/bit}$
 - On-chip communication: $\sim 100\text{GB/s}$ - 10TB/s , $0.1\text{-}1\text{ pJ/bit}$



PC system-level bus trends



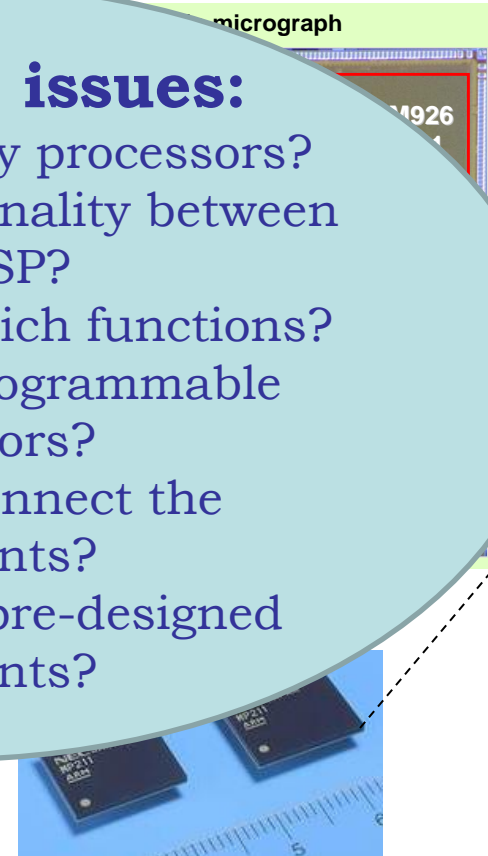
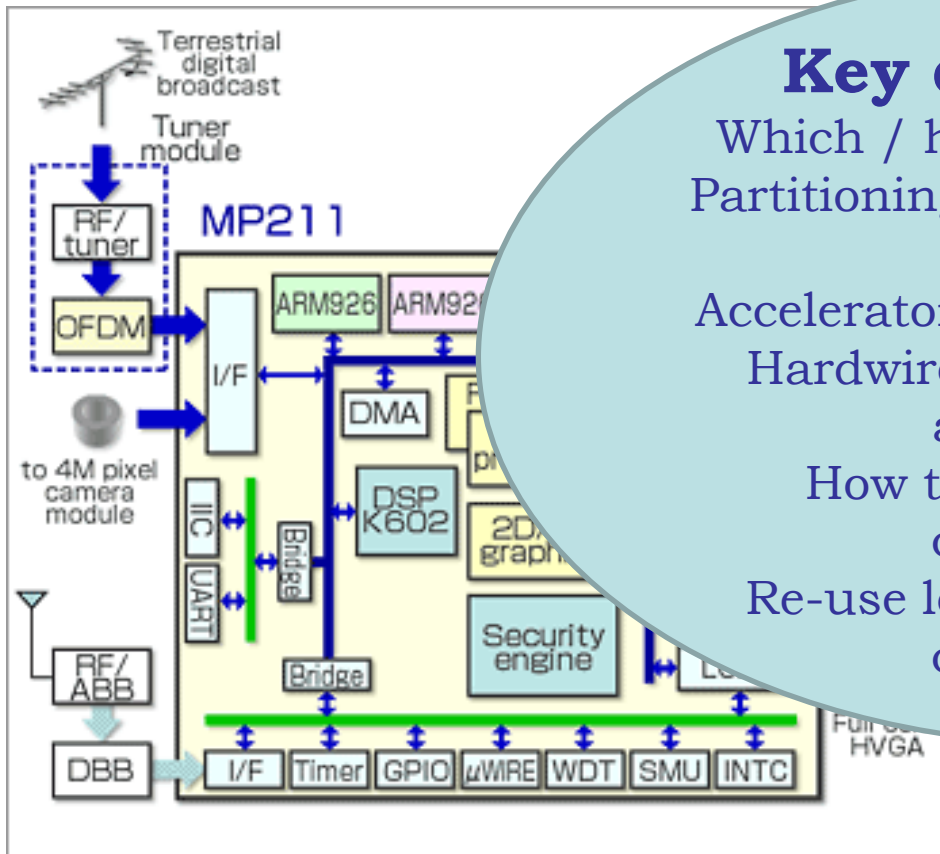
On-chip wire delay and power in 65nm technology (Source: Intel)

Key SoC Design Issues

- MP211: Multi-core mobile phone SoC
 - 3 ARM CPUs, VLIW DSP, Programmable Security Processor, 2D/2D graphics accelerator, Image processor, DDR/LCD/SD/MS interfaces, peripherals

Key design issues:

Which / how many processors?
Partitioning functionality between CPU, DSP?
Accelerators for which functions?
Hardwired vs. programmable accelerators?
How to interconnect the components?
Re-use legacy / pre-designed components?



Objective of this Course

- To give students an understanding and appreciation of the central design issues in SoC architecture, and hands-on experience with addressing some of them
- Design above the Register-transfer Level
- Designing systems that contain a mix of Digital Hardware and Software

How does this fit-in with other Purdue ECE courses?

- ECE 559 (MOS VLSI Design)
 - Design at the transistor-level
- ECE 670K (Modeling and Optimization of High Performance Interconnects)
 - Physical design (placement, routing, clock tree synthesis)
- ECE 595Z (Digital Logic Synthesis)
 - From register-transfer level to gates
 - Emphasis on automation (how the tools work)

This class addresses design at a different level of abstraction (what happens before logic/physical design?)

- ECE 565 (Computer Architecture)
 - Focuses on how to design a micro-processor

In this class, the processor will be used as a component to design larger systems

Topics / Schedule (Tentative)

- Introduction (this lecture)
- Background (IC design flow, levels of abstraction), Quick tour through SoC design process (1 lecture)
- Hardware/Software Partitioning and Co-Design (6 lectures)
 - The tradeoff between efficiency and flexibility
 - Designing hardware accelerators, Interfacing accelerators to software, Automatic HW/SW Partitioning
 - Application-specific Instruction Processors, Basic approaches to ASIP design, Extensible processors, Automatic synthesis of custom instruction sets
 - Efficient software architectures for hardware acceleration
- Modeling and Co-Simulating Hardware and Software (2 lectures)
 - Modeling abstractions for hardware (FSM+Datapath, cycle-accurate functional, behavioral), Modeling abstractions for programmable processors (Instruction-set simulation, compiled simulation), HW/SW co-simulation

Topics / Schedule (contd.)

- On-chip Communication Architecture Design (6 lectures)
 - Interconnect scaling challenges, on-chip buses – concepts and real examples, Optimizing bus-based communication architectures, Networks-on-chip
- Behavioral Synthesis: Compiling software into hardware (6 lectures)
 - Steps involved in behavioral synthesis, Scheduling, Resource sharing/binding, Advanced performance and power optimization techniques
- Design Re-use: Core-based and Platform-based Design (2 lectures)
- Advanced / current research topics (2 lectures)

Grading

- 40% - Homework/Lab Assignments
- 30% - Course Project
- 20% - Midterm
- 10% - Class participation

- Late submissions: -20% per day

Homework/Lab Assignments

- HW1: 1-page introduction to yourself
- HW2: Introduction to the Altera Embedded Development Suite and DE2 FPGA platform
 - Build a simple system-on-chip using Altera SOPC Builder, generate RTL and synthesize to the FPGA, develop and run a simple test program on the DE2 board
- HW3: Designing a simple HW accelerator and integrating it into an SoC
 - Tools: Altera DE3 Board, SOPC Builder, NiosII Software IDE

Homework/Lab Assignments (contd.)

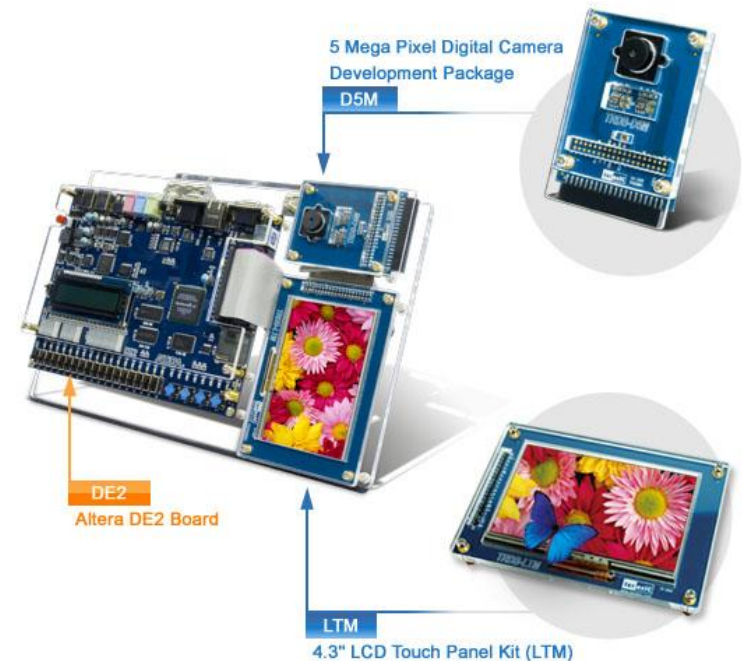
- HW4: Designing custom instructions to accelerate a program
 - Tools: Altera DE3 Board, SOPC Builder, NiosII Software IDE
- HW5: HW/SW co-simulation
 - Specify hardware using the FSMD model and co-simulate with an ISS
 - Tools: Gezel hardware modeling framework, Simit-ARM Instruction Set Simulator
- HW6: C-to-Hardware synthesis
 - Tools: Mentor Graphics Catapult C

Design Challenge (Course Project)

- Design HW/SW architecture for an application of moderate complexity
 - Working prototype demonstrated at the end of the semester
 - Emphasis on architecture exploration / optimized designs, not just any working system
- Option 1: Standard (very likely to be JPEG decoder)
- Option 2: Pick your own application (requires a proposal and discussion with me)
 - Must be of right complexity (not too easy, not too tough), interesting, and not available online ☺

Design Challenge : Platform

- Altera
 - DE2 FPGA board
 - SOPC builder
 - NiosII Configurable Soft Processor
 - NiosII Software Integrated Development Environment
 - Optional: Digital Camera, LCD touch panel



Using the tools and FPGA platform

- The software tools for all homeworks and the project (including Altera tools) can be accessed from any Linux machine on the ECN network
 - E.g., Linux PCs in MSEE189/190
- Using the Altera DE2 FPGA board requires you to physically go to the lab
- EE69 (basement of EE building, next to vending machines)
 - Requires access code, I will arrange for you to receive this

Lab usage guidelines

- We will be sharing the lab with ECE437L (undergraduate computer architecture prototyping lab)
 - 437L students get priority of access during their scheduled lab sections and office hours
 - First-come-first-serve at all other times
- Please see ECE437L schedule page for lab section and office hour times (will be updated over next 2 weeks)
 - <http://cobweb.ecn.purdue.edu/~ece437l/schedule>
- Please see ECE437L syllabus (Section 12, EE69 Lab Rules) for general guidelines
 - <http://cobweb.ecn.purdue.edu/~ece437l/syllabus/>

Expected Background

- Hardware
 - Digital logic design, HW design using HDL and synthesis/simulation tools*, some exposure to FPGA prototyping*
- Software - C programming, write and debug programs of moderate complexity
- Comfortable with using and programming on Linux/UNIX computing platforms
- Above all, willingness to
 - Challenge yourself and go beyond your comfort zone
 - Put in the extra time to fill any gaps in background

If you do not have background in HDL-based HW Design

- Please consider attending the first 5-6 weeks of lectures for ECE 337 ASIC Design
- T-Th, 9:30-10:20, ME 1052
- Please let Dr. Mark Johnson know that you are a student from ECE 695R

Expectations

- This is a hands-on class, be prepared to implement and debug HW/SW systems of moderate complexity
- You will be using industrial tools and hardware platforms, without much hand-holding
 - Extensive documentation available, but ability to zoom in on what is relevant is critical
 - Strongly encouraged to collaborate and exchange information on tools / FPGA platform / debugging
 - However, actual labs and project should be your own effort
- Great opportunity to go beyond the minimum (learn and use advanced design techniques push the limits of tools and hardware platform)

Reference Material

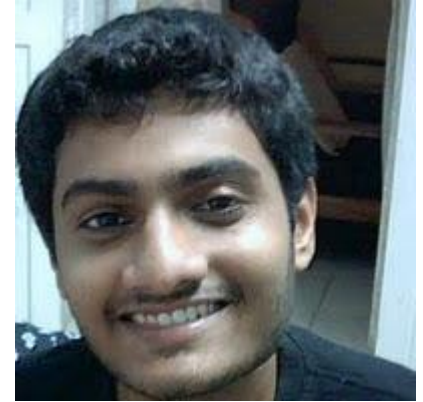
- Course Notes and Handouts
 - Primary source of information
- Significant online resources (manuals / documentation) will be provided for the assignments and project
- Unfortunately, there is no good textbook for this topic

Reference Books

- Reference Books – in no particular order (click on titles for hyperlinks)
 - Introduction to SoCs and Embedded Systems
 - [Computers as Components: Principles of Embedded Computing System Design](#), Wolf
 - [Embedded System Design: A Unified Hardware/Software Introduction](#), Vahid, Givargis (early edition available online)
 - [Multiprocessor Systems-on-chips](#), Jerraya/Wolf
 - [Surviving the SOC Revolution - A Guide to Platform-Based Design](#), Chang/Todd/Nelly/Martin/Cooke
 - [Winning the SoC Revolution: Experiences in Real Design](#), Martin/Chang (Editors)
 - HW/SW Co-Design
 - [Hardware/Software Co-Design - Principles and Practice](#), Straunstrup / Wolf
 - [Readings in Hardware/Software Co-Design](#), De Micheli / Ernst / Wolf
 - Custom Processors and ASIPs
 - [Processor Design: System-On-Chip Computing for ASICs and FPGAs](#), Nurmi (Editor)
 - [Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors](#), Rowen
 - [Customizable Embedded Processors: Design Technologies and Applications](#), Ienne / Leupers
 - On-chip Communication Architecture
 - [On-Chip Communication Architectures: System on Chip Interconnect](#), Pasricha/Dutt
 - [Networks on Chips: Technology and Tools](#), De Micheli/Benini
 - Behavioral Synthesis
 - [High-level Synthesis: Introduction to Chip and System Design](#), Gajski/Dutt/Wu/Lin
 - [Synthesis and Optimization of Digital Circuits](#), De Micheli

TA

- Hrishikesh Jayakumar
(hjayakum@purdue.edu)
- TA office hours (in the EE 69 lab):
Monday, Thursday 11AM-1PM
- Acknowledgement: Harris Corporation



Administrivia

- Office hours: Tuesday, Thursday 2:30PM – 3:30PM
 - If you need to talk to me outside office hours, please feel free to ask (right before class NOT a good time)
- Course material, announcements, homework submissions using Blackboard & email list
 - Lecture material will be posted after each class
- Assistant: Bonnie Misner
 - Office: MSEE 330, Email: misner@purdue.edu
- Travel: I may have to miss 1 or 2 classes due to conference travel
 - Will co-ordinate makeup classes if necessary

Contingency Preparation

- In the event of a major campus emergency, course requirements, deadlines and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances. In such an event, information will be provided through Blackboard.

Did You Know?

- The integrated circuit was first conceived by Geoffrey W. A. Dummer (British Ministry of Defense) and published on May 7th, 1952. He unsuccessfully attempted to build such a circuit in 1956.
- The IC was first realized by Jack Kilby (Texas Instruments) and Robert Noyce (Fairchild Semiconductor) around the same time.
- Kilby built a working prototype by Sept. 1958, and TI filed a patent on Feb. 6th, 1959
- Robert Noyce came up with his idea for an integrated circuit ~6 months after Kilby. His invention solved the problem of interconnecting the components by adding a metal layer
- Knowing that TI had already filed a patent on something similar, Fairchild wrote out a highly detailed application, hoping that it wouldn't infringe on TI 's similar device.
- All that detail paid off. On April 25, 1961, the patent office awarded the first patent for an integrated circuit to Robert Noyce while Kilby's application was still being analyzed. Today, both men are acknowledged as having independently conceived of the idea.
- Noyce went on to be a co-founder of Intel.
- Kilby was jointly awarded the Nobel Prize in Physics in 2000.



Geoffrey Dummer



Jack Kilby



Robert Noyce

Source: nobelprize.org, pbs.org